We have three private **direct-mapped** caches connected to three processors. Each cache has 4 lines, with 2 words each. The system is word addressable, with 2^4 addressable words.

The caches are **write-back** upon eviction, and **write-allocate**. They implement the **MSI** snooping protocol given on the next page. Assume atomic and sequential operations.

You are given the initial contents of memory. Calculate the final state of cache and memory as a result of running the pseudocode given on this page. ***Write the final contents of cache and memory in the space provided on the next page.***

P1	Address	Tag (1 bit)	XXX0 (data)	XXX1 (data)	State (M,S,I)
	X00X				
	X01X				
	X10X				
	X11X				

P2	Address	Tag (1 bit)	XXX0 (data)	XXX1 (data)	State (M,S,I)
	X00X				
	X01X				
	X10X				
	X11X				

P3	Address	Tag (1 bit)	XXX0 (data)	XXX1 (data)	State (M,S,I)
	X00X				
	X01X				
	X10X				
	X11X				

Memory

0000	16
0001	24
0010	-8
0011	-9
0100	10
0101	12
0110	87
0111	3
1000	26
1001	19
1010	-103
1011	4
1100	77
1101	98
1110	91
1111	92

Instructions:

P1 0000 = 1110 + 0000
P2 1101 = 0000 + 0010
P3 0000 = 1001 + 1010
P1 0101 = 1001 + 0000

Put the final state here:

	Address	Tag (1 bit)	XXX0 (data)	XXX1 (data)	State (M,S,I)
P1	X00X				
	X01X				
	X10X				
	X11X				

	Address	Tag (1 bit)	XXX0 (data)	XXX1 (data)	State (M,S,I)
P2	X00X				
	X01X				
	X10X				
	X11X				

	Address	Tag (1 bit)	XXX0 (data)	XXX1 (data)	State (M,S,I)
P3	X00X				
	X01X				
	X10X				
	X11X				

Memory

0000	
0001	
0010	
0011	
0100	
0101	
0110	
0111	
1000	
1001	
1010	
1011	
1100	
1101	
1110	
1111