CmpSci 535 VLSI Cost Model

$$\text{Cost}_{\text{IC}} = \frac{\text{Cost}_{\text{chip}} + \text{Cost}_{\text{test}} + \text{Cost}_{\text{package}}}{\text{Yield}_{\text{final}}}$$

$\text{Cost}_{\text{package}}$ and $\text{Yield}_{\text{final}}$ are given. Others must be computed.

$$\text{Cost}_{\text{chip}} = \frac{\text{Cost}_{\text{wafer}}}{\text{Chips}_{\text{wafer}} \times \text{Yield}_{\text{die}}}$$

$\text{Cost}_{\text{wafer}}$ is the total cost for the fabricated wafer and is given.

$$\text{Chips}_{\text{wafer}} = \left\lfloor \frac{\pi \times \left(\frac{\text{Diameter}_{\text{wafer}}}{2}\right)^2}{\text{Area}_{\text{chip}}} - \frac{\pi \times \text{Diameter}_{\text{wafer}}}{\sqrt{2 \times \text{Area}_{\text{chip}}}} - \text{TestSites}_{\text{wafer}} \right\rfloor$$

$\text{Diameter}_{\text{wafer}}$ is 200mm or 300mm (450mm may be in the future). $\text{Area}_{\text{chip}}$ is given, or calculated from chip dimensions. $\text{TestSites}_{\text{wafer}}$ is the number of chip sites devoted to testing. This is usually 0 in a production process, but may be a small integer for a prototyping run.

$$\text{Yield}_{\text{die}} = \text{Yield}_{\text{wafer}} \times \left(1 + \frac{\text{Defects}_{\text{unit-area}} \times \text{Area}_{\text{chip}}}{\text{P}}\right)^{-\text{P}}$$

$\text{Yield}_{\text{wafer}}$ is the given fraction of good wafers (usually very close to 1). $\text{Defects}_{\text{unit-area}}$ is also given, and depends on the process. P is an empirically determined factor to account for the complexity of a process.

$$\text{Cost}_{\text{test}} = \frac{\text{Cost}_{\text{hour}} \times \text{Time}_{\text{test}}}{\text{Yield}_{\text{die}}}$$

$\text{Cost}_{\text{hourr}}$ is the cost per hour for running tests.