For each of these exercises, assume a very tiny cache with 16 lines of two words each, and a main memory address space of 8 bits:

Tag	Index	Word 1	Word 0
	0000		
	0001		
	0010		
	0011		
	0100		
	0101		
	0110		
	0111		
	1000		
	1001		
	1010		
	1011		
	1100		
	1101		
	1110		
	1111		

The processor executes a program that accesses memory in the following sequence of addresses:

00000000	10001110	01100101
00000001	10001111	01110101
00000010	00000000	01000101
00000011	00000101	11100101
00000100	00000011	01100101
00000101	00000110	00000101
00000110	10001000	00010101
00000111	10001001	10000101
10001000	00110001	11000111
10001001	00110011	11001000
10001010	00110110	11001001
10001011	00110111	11101000
10001100	00111000	
10001101	00101010	

Determine the hit rate if the cache is direct-mapped. Mark each reference that is a hit as H, compulsory miss as C, and conflict miss as X.

Tag	Set Index	Word 1	Word 0	LRU
	000			
	000			
	001			
	001			
	010			
	010			
	011			
	011			
	100			
	100			
	101			
	101			
	110			
	110			
	111			
	111			

The processor executes a program that accesses memory in the following sequence of addresses:

00000000	10001110	01100101
00000001	10001111	01110101
00000010	00000000	01000101
00000011	00000101	11100101
00000100	00000011	01100101
00000101	00000110	00000101
00000110	10001000	00010101
00000111	10001001	10000101
10001000	00110001	11000111
10001001	00110011	11001000
10001010	00110110	11001001
10001011	00110111	11101000
10001100	00111000	
10001101	00101010	

Determine the hit rate if the cache is 2-way set associative with LRU replacement. Mark each reference that is a hit as H, compulsory miss as C, and conflict miss as X.

Tag	Set Index	Word 1	Word 0	LRU
	00			
	00			
	00			
	00			
	01			
	01			
	01			
	01			
	10			
	10			
	10			
	10			
	11			
	11			
	11			
	11			

The processor executes a program that accesses memory in the following sequence of addresses:

00000000	10001110	01100101
00000001	10001111	01110101
00000010	00000000	01000101
00000011	00000101	11100101
00000100	00000011	01100101
00000101	00000110	00000101
00000110	10001000	00010101
00000111	10001001	10000101
10001000	00110001	11000111
10001001	00110011	11001000
10001010	00110110	11001001
10001011	00110111	11101000
10001100	00111000	
10001101	00101010	

Determine the hit rate if the cache is 4-way set associative with LRU replacement. Mark each reference that is a hit as H, compulsory miss as C, and conflict miss as X.

Tag	Word 1	Word 0	LRU

The processor executes a program that accesses memory in the following sequence of addresses:

00000000	10001110	01100101
00000001	10001111	01110101
00000010	00000000	01000101
00000011	00000101	11100101
00000100	00000011	01100101
00000101	00000110	00000101
00000110	10001000	00010101
00000111	10001001	10000101
10001000	00110001	11000111
10001001	00110011	11001000
10001010	00110110	11001001
10001011	00110111	11101000
10001100	00111000	
10001101	00101010	

Determine the hit rate if the cache is fully associative with LRU replacement. Mark each reference that is a hit as H, compulsory miss as C, and conflict miss as X.

Tag	Index	Word 1	Word 0
	0000		
	0001		
	0010		
	0011		
	0100		
	0101		
	0110		
	0111		
	1000		
	1001		
	1010		
	1011		
	1100		
	1101		
	1110		
	1111		

Tag	Index	Word 1	Word 0	LRU	V	D

The processor executes a program that accesses memory in the following sequence of addresses:

00000000	10001110	01100101
00000001	10001111	01110101
00000010	00000000	01000101
00000011	00000101	11100101
00000100	00000011	01100101
00000101	00000110	00000101
00000110	10001000	00010101
00000111	10001001	10000101
10001000	00110001	11000111
10001001	00110011	11001000
10001010	00110110	11001001
10001011	00110111	11101000
10001100	00111000	
10001101	00101010	

Determine the hit rate if the cache is direct-mapped with a two-entry victim buffer. A hit in the victim buffer counts as a hit. The line in the victim buffer and the cache are swapped. The victim buffer is fully associative, with LRU replacement. Mark each reference that is a hit as H, compulsory miss as C, and conflict miss as X, victim hit as V.

Tag	Set Index	Word 1	Word 0	LRU	V	D
	00					
	00					
	00					
	00					
	01					
	01					
	01					
	01					
	10					
	10					
	10					
	10					
	11					
	11					
	11					
	11					

Tag	Set Index	Word 1	Word 0	LRU	V	D

The processor executes a program that accesses memory in the following sequence of addresses:

00000000	10001110	01100101
00000001	10001111	01110101
00000010	00000000	01000101
00000011	00000101	11100101
00000100	00000011	01100101
00000101	00000110	00000101
00000110	10001000	00010101
00000111	10001001	10000101
10001000	00110001	11000111
10001001	00110011	11001000
10001010	00110110	11001001
10001011	00110111	11101000
10001100	00111000	
10001101	00101010	

Determine the hit rate if the cache is 4-way set associative with a two-line victim buffer, both with LRU replacement, and mark each reference that is a hit. Mark misses as compulsory (C) or conflict (X). Distinguish between victim buffer hits (V) and regular hits (H).