CmpSci 535 Sample Midterm Name _____

This exam is open book and notes. A calculator is needed for some of the problems.

1. How does a one-address architecture operate?

2. Explain the difference between register direct and register indirect addressing.

3. In PC-relative immediate addressing, why is the immediate offset sign-extended before being added?

4. What is the disadvantage of the single-instruction Test-and-Branch approach with respect to having branches check a condition that is set by a previous instruction?

5. Give a disadvantage of designing a three-address architecture to have 256 registers.

6. Why is it important to be able to turn off interrupts?

7. a. Given an 8-stage pipeline like the MIPS that we saw in class, where the stages are IF, IS, RF, EX DF, DS, TC, WB, and given the following instruction sequence, show how to reorder the sequence to avoid at least one existing stall.

		Reordered instructions:
load R7, X	// R7 = memory[X]	_____
sub R2, R0, R7	// R2 = -R7 (R0 is constant 0)	_____
mul R5, R2, 10	// R5 = R2 * immediate value 10	_____
store X, R5	// memory[X] = R5	_____
load R22, Y	// R22 = memory[Y]	_____
sub R22, R0, R22	// R22 = -R22	_____

7. b. Show the flow of the reordered instructions through the pipe, using the following grid. Mark stalls D for data and S for structural. Show the stage that each instruction is in using the stage names above. The first stage for the first instruction is already shown.

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
IF																															

7. c. What is the efficiency of the pipeline running the reordered instruction sequence?

8. Why does the tag field of a cache shrink as the line length increases?

9. Why does a cache line need a dirty bit?

10. The data cache shown below is direct mapped and has a one-element victim buffer. Show its **contents** after executing the following memory trace that contains the addresses from read operations, given the contents of memory shown in the box to the right to the trace. Also, mark each reference as either a cache hit (H), a victim buffer hit (V), or a compulsory miss (R) or a conflict miss (C). The cache has its initial contents shown.

Tag	Line#	Word 00	Word 01	Word10	Word11
0	00	01	06	12	04
1	01	19	14	07	23
1	10	44	28	39	32
0	11	02	18	13	09
100	VB	03	08	17	15

Memory Address Trace	Hit/Miss Type
10000	____
00001	____
11001	____
00100	____
01011	____
00001	____

Address	Contents (Decimal)
00000	01
00001	06
00010	12
00011	04
00100	21
00101	20
00110	00
00111	11
01000	05
01001	22
01010	16
01011	10
01100	02
01101	18
01110	13
01111	09
10000	03
10001	08
10010	17
10011	15
10100	19
10101	14
10110	07
10111	23
11000	44
11001	28
11010	39
11011	32

11. Each part of question 11 refers to the same chip and fabrication process. Show your work.
    a. Processor chips with dimensions of 11 mm by 14.5 mm are being manufactured on a 300 mm diameter wafer. How many whole chips fit on this wafer? (There are no test sites.)

11. b. If the $Yield_{Wafer}$ is 0.998, $Defects_{unit\text{-}area}$ is 0.7/cm^2, and P is 4.5, what is $Yield_{die}$?

11. c. If $Cost_{wafer}$ = \$7300, what is $Cost_{chip}$?

11. d. If $Cost_{test}$ = \$4.50 and $Cost_{package}$ = \$5.25, and $Yield_{final}$=0.99 what is $Cost_{IC}$?

11. e. If the processor accounts for 7% of system cost, what will be the cost of a system using this chip?

12. Give an example of a recurring cost in manufacturing integrated circuits.

13. Why is a string move operation not appropriate for a RISC architecture? Explain in terms of separability and schedulability of operations.